

What is claimed is:

1. A step-up circuit, comprising:
a step-up clock signal generation device that generates a clock signal to be used for voltage step-up;

5 a plurality of step-up stages for successively stepping up a power supply voltage based on the clock signal; and

a control device that controls, after starting an operation, the clock signal generated by the step-up clock signal generation device to be supplied to the plurality of step-up stages at different timings.

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2. A step-up circuit according to claim 1, wherein the step-up clock signal generation device generates a clock signal to be used for voltage step-up based on a clock signal applied, and

wherein the control device includes:

15 a counter that counts the clock signal applied to the step-up clock signal generation circuit, and

a plurality of output control circuits that respectively supply, based on different output values of the counter, the clock signal generated by the step-up clock signal generation circuit to the plurality of step-up stages.

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3. A step-up circuit according to claim 1, wherein the control device includes:
a counter that counts pulse signals applied, and

a plurality of output control circuits that respectively supply, based on different output values of the counter, the clock signal generated by the step-up clock signal generation circuit to the plurality of step-up stages.

5 4. A step-up circuit, comprising:

a step-up clock signal generation circuit that generates a clock signal to be used for voltage step-up;

a plurality of step-up stages that successively step up a power supply voltage based on the clock signal; and

10 a control device that, after a start of operation, activates the plurality of step-up stages at different timings.

5. A step-up circuit according to claim 4, wherein the step-up clock signal generation device generates a clock signal to be used for voltage step-up based on a clock signal applied,

15 and

wherein the control device includes:

a counter that counts the clock signal applied to the step-up clock signal generation circuit,

wherein the plurality of output stages are activated based on different output values of
20 the counter.

6. A step-up circuit according to claim 4, wherein the control device includes:

a counter that counts pulse signals applied, wherein the plurality of step-up stages are activated based on different output values of the counter.

7. A step-up circuit, comprising:

5 a step-up clock signal generation device that generates a clock signal to be used for voltage step-up;

at least one step-up stage that steps up a power supply voltage based on the clock signal; and

a control device that, after starting an operation, changes a frequency of the clock
10 signal to be supplied to the step-up stage from a value lower than a normal value to the normal value.

8. A step-up circuit according to claim 7, wherein the control device includes:

a plurality of frequency-divider circuits that frequency-divide the clock signal
15 generated by the step-up clock signal generation device, and respectively output a plurality of divided clock signals having different frequency division ratios,

a selector circuit that selects, based on a control signal, one of the clock signal and the plurality of frequency-divided clock signals, and

a counter that counts the clock signal selected by the selector circuit to thereby
20 generate the control signal; and

wherein the step-up stage steps up the power supply voltage based on the clock signal selected by the selector circuit.

9. A step-up circuit according to claim 7, wherein the control device includes:

a plurality of frequency-divider circuits that frequency-divide a clock signal applied, and respectively output a plurality of divided clock signals having different frequency division ratios,

5 a selector circuit that selects, based on a control signal, one of the clock signal and the plurality of frequency-divided clock signals, and

a counter that counts the clock signal selected by the selector circuit to thereby generate the control signal; and

wherein the step-up clock signal generation circuit generates, based on the clock
10 signal selected by the selector circuit, a clock signal to be used for voltage step-up.

10. A step-up circuit according to claim 7, wherein the control device includes:

a plurality of frequency-divider circuits that frequency-divide a clock signal applied, and respectively output a plurality of frequency-divided clock signals having different
15 frequency division ratios,

a counter that counts pulse signals applied, and

a selector circuit that selects, based on an output value of the counter, one of the clock signal and the plurality of frequency-divided clock signals; and

wherein the step-up clock signal generation circuit generates, based on the clock
20 signal selected by the selector circuit, a clock signal to be used for voltage step-up.

11. A step-up circuit, comprising:

means for generating a step-up clock signal to be used for voltage step-up;

means for successively stepping up a power supply voltage based on the clock signal;
and

means for controlling, after starting an operation, the clock signal generated by the
means for generating a step-up clock signal to be supplied to the means for successively
5 stepping up at different timings.

12. A step-up circuit according to claim 11, wherein the means for generating a
step-up clock signal generates a clock signal to be used for voltage step-up based on a clock
signal applied, and

10 wherein the means for controlling includes:

means for counting the clock signal applied to the step-up clock signal generation
circuit, and

a plurality of output control circuits that respectively supply, based on different
output values of the means for counting, the clock signal generated by the step-up clock
15 signal generation circuit to the means.

13. A step-up circuit according to claim 11, wherein the means for controlling
includes:

means for counting pulse signals applied, and

20 a plurality of output control circuits that respectively supply, based on different
output values of the means for counting, the clock signal generated by the step-up clock
signal generation circuit to the means for successively stepping up.

14. A step-up circuit, comprising:

means for generating a step-up clock signal to be used for voltage step-up;

means for successively stepping up a power supply voltage based on the clock signal;

and

5 means for controlling that, after a start of operation, activates the means for successively stepping up at different timings.

15. A step-up circuit according to claim 14, wherein the means for generating a step-up clock signal generates a clock signal to be used for voltage step-up based on a clock

10 signal applied, and

wherein the means for controlling includes:

means for counting the clock signal applied to the step-up clock signal generation circuit,

wherein the plurality of output stages are activated based on different output values of
15 the means for counting.

16. A step-up circuit according to claim 14, wherein the means for controlling includes:

means for counting pulse signals applied, wherein the means for successively
20 stepping up are activated based on different output values of the means for counting.

17. A step-up circuit, comprising:

means for generating a step-up clock signal to be used for voltage step-up;

means for successively stepping up a power supply voltage based on the clock signal;
and

a means for controlling that, after starting an operation, changes a frequency of the clock signal to be supplied to the means for successively stepping up from a value lower than
5 a normal value to the normal value.

18. A step-up circuit according to claim 17, wherein the means for controlling includes:

means for frequency-dividing the clock signal generated by the means for generating
a step-up clock signal, and respectively output a plurality of divided clock signals having
10 different frequency division ratios,

means for selecting, based on a control signal, one of the clock signal and the
plurality of frequency-divided clock signals, and

means for counting the clock signal selected by the means for selecting to thereby
generate the control signal; and

15 wherein the means for successively stepping up steps up the power supply voltage
based on the clock signal selected by the means for selecting.

19. A step-up circuit according to claim 17, wherein the means for controlling includes:

means for frequency-dividing the clock signal a clock signal applied, and respectively
20 output a plurality of divided clock signals having different frequency division ratios,

means for selecting, based on a control signal, one of the clock signal and the
plurality of frequency-divided clock signals, and

means for counting the clock signal selected by the means for selecting to thereby generate the control signal; and

wherein the means for successively stepping up generates, based on the clock signal selected by the means for selecting, a clock signal to be used for voltage step-up.

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20. A step-up circuit according to claim 17, wherein the means for controlling includes:

means for frequency-dividing the clock signal a clock signal applied, and respectively output a plurality of frequency-divided clock signals having different frequency division ratios,

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means for counting pulse signals applied, and
means for selecting, based on an output value of the means for counting, one of the clock signal and the plurality of frequency-divided clock signals; and

wherein the means for successively stepping up generates, based on the clock signal selected by the means for selecting, a clock signal to be used for voltage step-up.

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21. A method of operating a step-up circuit, comprising:

generating a step-up clock signal to be used for voltage step-up;

successively stepping up a power supply voltage based on the clock signal; and

controlling, after starting an operation, the clock signal generated at different timings.

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22. A method of operating a step-up circuit according to claim 21, wherein the generating a step-up clock signal generates a clock signal to be used for voltage step-up based on a clock signal applied, and

wherein the controlling includes:

counting the clock signal, and

supplying, based on different output values of the counting, the clock signal.

5 23. A method of operating a step-up circuit according to claim 21, wherein the
controlling includes:

counting pulse signals applied, and

supplying, based on different output values of the counting, the clock signal.

10 24. A method of operating a step-up circuit, comprising:
generating a step-up clock signal to be used for voltage step-up;
successively stepping up a power supply voltage based on the clock signal; and
after a start of operation, successively stepping up at different timings.

15 25. A method of operating a step-up circuit according to claim 24, wherein the
generating a step-up clock signal generates a clock signal to be used for voltage step-up
based on a clock signal applied, and

wherein the successively stepping up at different timings includes:

counting the clock signal applied to the step-up clock signal generation circuit,

20 activating the plurality of output stages based on different output values of the
counting.

26. A method of operating a step-up circuit according to claim 24, wherein the successively stepping up at different timings includes:

counting pulse signals applied.

5 27. A method of operating a step-up circuit, comprising:
generating a step-up clock signal to be used for voltage step-up;
successively stepping up a power supply voltage based on the clock signal; and
changing, after starting an operation, a frequency of the clock signal to be supplied to
the successively stepping up from a value lower than a normal value to the normal value.

10 28. A method of operating a step-up circuit according to claim 27, wherein the changing includes:

frequency-dividing the clock signal generated by the generating a step-up clock
signal, and respectively outputting a plurality of divided clock signals having different

15 frequency division ratios,

selecting, based on a control signal, one of the clock signal and the plurality of
frequency-divided clock signals, and

counting the clock signal selected by the selecting to generate the control signal; and
wherein the successively stepping up steps up the power supply voltage based on the
20 clock signal selected.

29. A method of operating a step-up circuit according to claim 27, wherein the changing includes:

frequency-dividing the clock signal applied, and respectively outputting a plurality of divided clock signals having different frequency division ratios,

selecting, based on a control signal, one of the clock signal and the plurality of frequency-divided clock signals, and

- 5 counting the clock signal selected to thereby generate the control signal; and
- wherein the successively stepping up generates, based on the clock signal selected, a clock signal to be used for voltage step-up.

30. A method of operating a step-up circuit according to claim 27, wherein the
- 10 changing includes:

 frequency-dividing the clock signal applied, and respectively outputting a plurality of frequency-divided clock signals having different frequency division ratios,

 counting pulse signals applied, and

- selecting, based on an output value of the counting, one of the clock signal and the
- 15 plurality of frequency-divided clock signals; and

 wherein the successively stepping up generates, based on the clock signal selected, a clock signal to be used for voltage step-up.